GENERAL DESCRIPTION

OB2279 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup design with OB2279. A large value resistor could thus be used in the startup circuit for reduced power loss.

The internal slope compensation improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle output.

Leading-edge blanking on current sense input removes the signal glitch due to snubber circuit diode reverse recovery and greatly reduces the external component count and system cost in the design.

OB2279 offers comprehensive protection coverage including Cycle-by-Cycle current limiting(OCP), VDD Under Voltage Lockout(UVLO), VDD Over Voltage Protection(OVP), VDD Clamp, Gate Clamp, Over Load protection(OLP) and Over Temperature protection (OTP), etc.

Different latch shutdown options are offered on OB2279 in different device version. V version has OVP Latch shutdown. T version supports both OVP and OTP latch shutdown. L version provides all OVP, OTP and OLP latch shutdown control.

Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique together with soft switching control at the totem pole gate drive output.

Tone energy at below 20KHZ is minimized in operation. Consequently, audio noise is eliminated during operation.

OB2279 is offered in SOP-8 and DIP-8 packages.

FEATURES

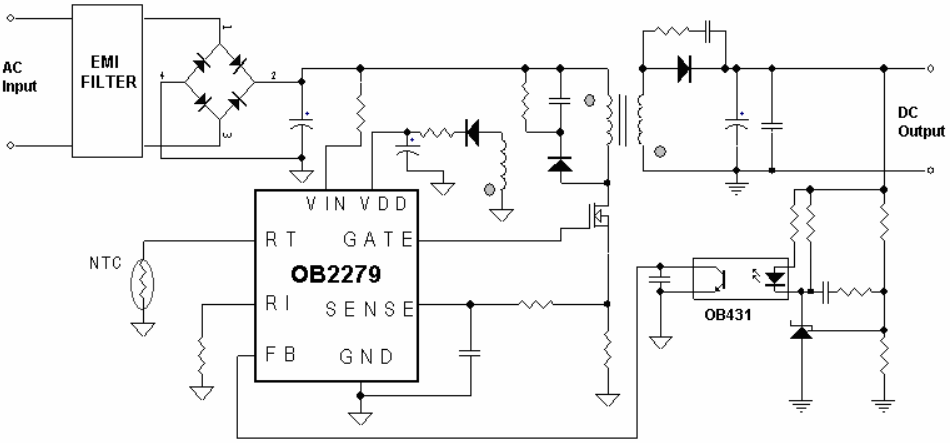
- On-Bright Proprietary Frequency Shuffling Technology for Improved EMI Performance
- Power On Soft Start
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- External Programmable PWM Switching Frequency
- Internal Synchronized Slope Compensation
- Low VIN/VDD Startup Current(3uA) and Low Operating Current (2.3mA)
- Leading Edge Blanking on Current Sense Input
- Complete Protection Coverage with selective protections for Latch Shutdown
  - VDD Over Voltage Protection(OVP) – Latch Shutdown
  - Over Temperature Protection(OTP) – Auto recovery or Latch Shutdown
  - Over Load Protection. (OLP) – Auto recovery or Latch Shutdown
  - VDD Under Voltage Lockout with Hysteresis (UVLO)
  - Gate Output Voltage Clamp (16.5V)
  - Built-in OCP Compensation to Achieve Minimum OPP Variation over Universal AC Input Range.

APPLICATIONS

Offline AC/DC flyback converter for

- Adaptor
- Notebook Adaptor
- LCD Monitor/TV/PC/Set-Top Box Power Supplies
- Open-frame SMPS
- Printer Power

TYPICAL APPLICATION



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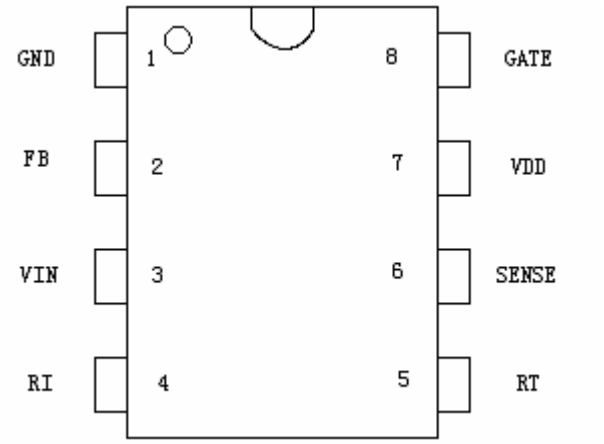
GENERAL INFORMATION

Pin Configuration

The pin map of OB2279 in DIP8 and SOP8 package is shown as below.



Ordering Information

Part Number	Description
OB2279AP-V	DIP8, V version with OVP Latch
OB2279AP-T	DIP8, T version with OVP/OTP latch
OB2279AP-L	DIP8, L version with OVP/OTP/OLP latch
OB2279CP-V	SOP8, V version with OVP latch
OB2279CP-T	SOP8, T version with OVP/OTP latch
OB2279CP-L	SOP8, L version with OVP/OTP/OLP latch

Note: All Devices are offered in Pb-free Package if not otherwise noted.

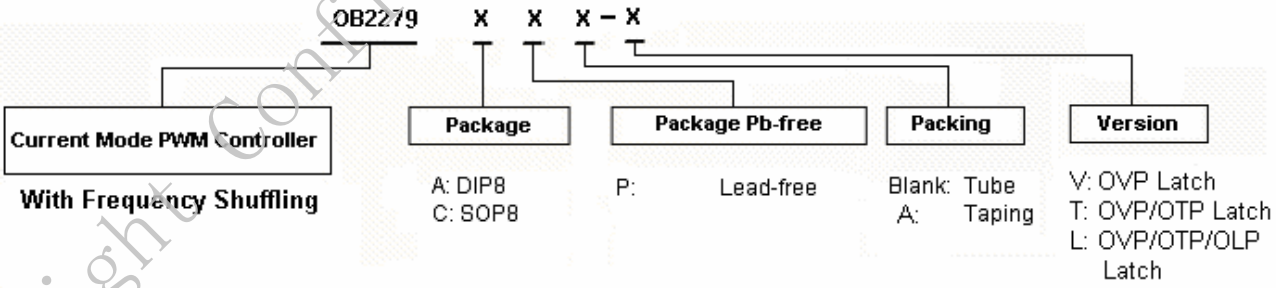
Package Dissipation Rating

Package	RθJA (°C/W)
DIP8	90
SOP8	150

Absolute Maximum Ratings

Parameter Value	
VDD Clamp Voltage	35 V
VDD Clamp Continuous Current	10 mA
V_{FB} Input Voltage	-0.3 to 7V
V_{SENSE} Input Voltage to Sense Pin	-0.3 to 7V
V_{RT} Input Voltage to RT Pin	-0.3 to 7V
V_{RI} Input Voltage to RI Pin	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-20 to 150 °C
Min/Max Storage Temperature T_{stg}	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



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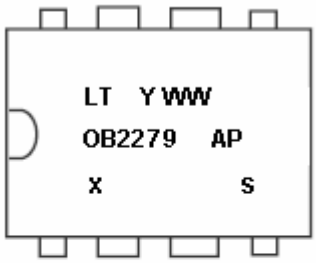
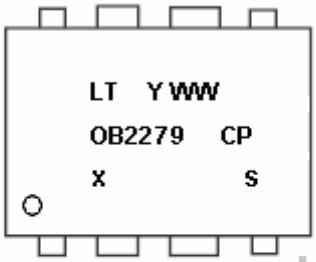
Marking Information

DIP8



A: DIP8 Package
P: Pb-free Package
Y: Year Code(0-9)
WW: Week Code(01-52)
X: Version
s: Internal Code

SOP8



C: SOP8 Package
P: Pb-free Package
Y: Year Code(0-9)
WW: Week Code(01-52)
X: Version
s: Internal Code

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1 GND		P	Ground
2	FB	I	Feedback input pin. PWM duty cycle is determined by voltage level into this pin and current-sense signal level at Pin 6.
3	VIN	I	Connected through a large value resistor to rectified line input for Startup and line voltage sensing.
4	RI	I	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
5	RT	I	Dual function pin. Either connected through a NTC resistor to GND for over temperature shutdown control or used as latch shutdown control input.
6	SENSE	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
7	VDD	P	DC power supply pin.
8	GATE	O	Totem-pole gate drive output for power MOSFET.

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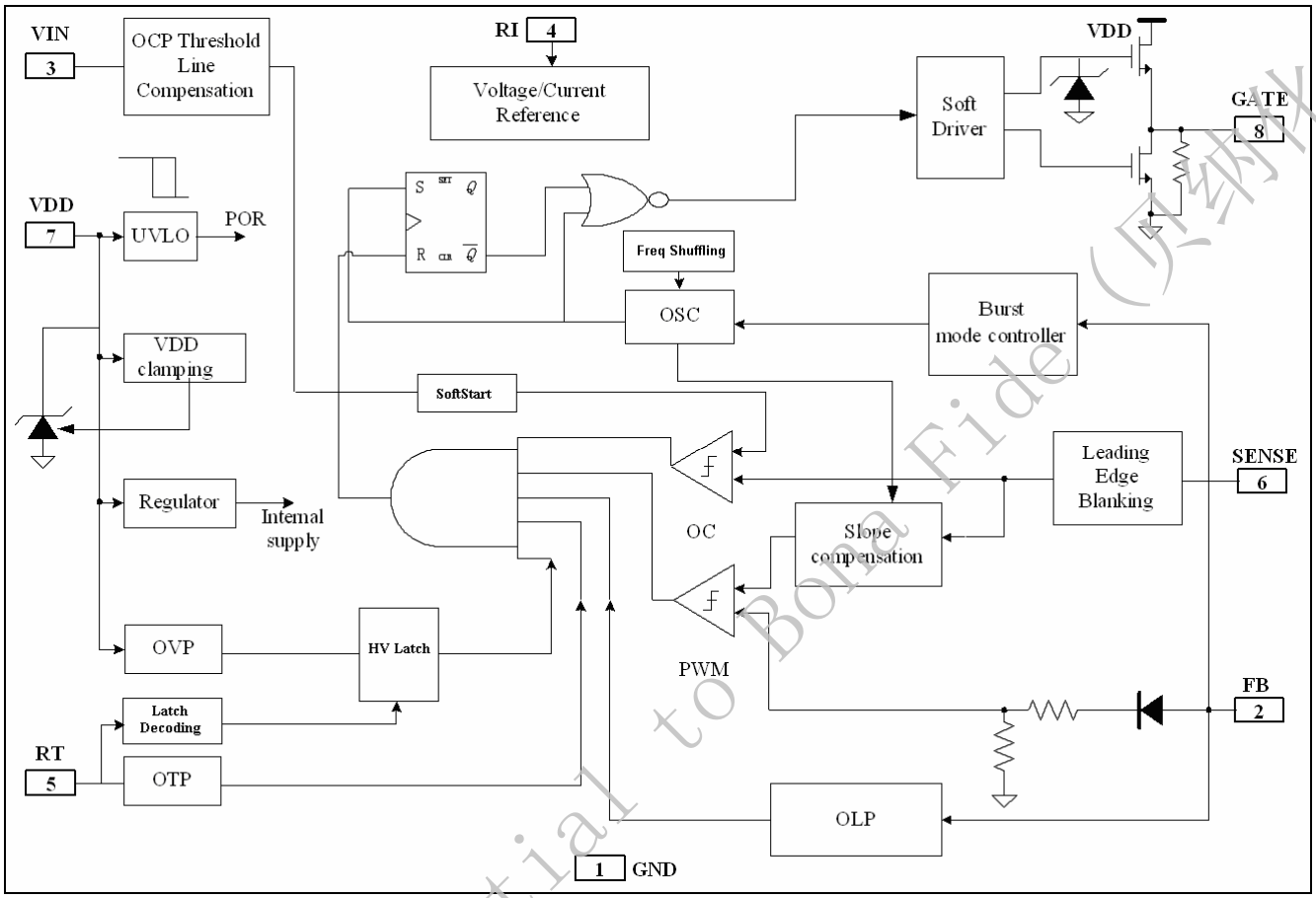
BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Max	Unit
VDD	VDD Supply Voltage	11.5	25	V
RI	RI Resistor Value	100	133	Kohm
T_A	Operating Ambient Temperature	-20	85	°C

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ELECTRICAL CHARACTERISTICS

(T_A = 25°C if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD)						
I_VDD_Startup	VDD Start up Current	VDD=15V, RI=100K Measure current into VDD	3		20	uA
I_VDD_Ops	Operation Current	VDD=16V, RI=100Kohm, V_{FB}=3V	2.3			mA
UVLO(Enter)	VDD Under Voltage Lockout Enter		8.8	9.8	10.8	V
UVLO(Exit)	VDD Under Voltage Lockout Exit (Startup)		15.5	16.5	17.5	V
OVP(Latch)	VDD Over Voltage Latch Trigger	26.5		28	29.5	V
OVP(De-Latch)	VDD Latch Release Voltage Threshold			7.5		V
I(Vdd)_latch	VDD bleeding current at latch shutdown when VDD = 9V			45		uA
T_D_OVP	VDD OVP Debounce time	RI = 100Kohm		80		uSec
V_{DD}_Clamp	V_{DD} Zener Clamp Voltage	RI = 100 Kohm, I(V_{DD}) = 5 mA	35			V
T_Softstart	Soft Start Time			3		mSec
Feedback Input Section(FB Pin)						
A_{VCS}	PWM Input Gain	$\Delta V_{FB} / \Delta V_{cs}$	2.8			V/V
V_{FB}_Open	V_{FB} Open Voltage	VDD = 16V		6.2	V	
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND, measure current	0.75			mA
V_{TH}_0D	Zero Duty Cycle FB Threshold Voltage	VDD = 16V, RI=100Kohm	0.95			V
V_{TH}_BM	Burst Mode FB Threshold Voltage			1.6		V
V_{TH}_PL	Power Limiting FB Threshold Voltage			4.4		V
T_D_PL	Power limiting Debounce Time	VDD = 16V, RI=100Kohm	80			mSec
Z_{FB}_IN	Input Impedance			9.0		Kohm
Current Sense Input(Sense Pin)						
T_blanking	Sense Input Leading Edge Blanking Time	RI = 100Kohm		300		nSec
Z_{SENSE}_IN	Sense Input Impedance			30		Kohm
T_D_OC	Over Current Detection and Control Delay	CL=1nf at GATE, RI=100Kohm	70			nSec
V_{TH}_OC_0	Current Limiting Threshold at No Compensation	VDD = 16V, I(VIN) = 0uA, RI=100Kohm	0.85	0.90	0.95	V

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V_{TH}_OC_1 Current	Limiting Threshold at Compensation	VDD = 16V, I(VIN) = 150uA, RI=100Kohm	0.80			V
Oscillator						
F_{OSC}	Normal Oscillation Frequency	RI = 100Kohm	60	65	70	KHZ
Δf_Temp	Central Frequency Temperature Stability	VDD = 16V, RI=100Kohm, -20°C to 100 °C	3			%
Δf_VDD	Central Frequency Voltage Stability	VDD = 12-28V, RI=100Kohm	3			%
RI_range	Operating RI Range		50	100	250	Kohm
V_RI_open	RI open voltage	VDD = 16V		2.0		V
F_BM	Burst Mode Base Frequency	VDD = 16V, RI=100Kohm	20			KHZ
Gate Drive Output						
VOL	Output Low Level	VDD = 16V, Io = 20 mA			0.3	V
VOH	Output High Level	VDD = 16V, Io = 20 mA	11			V
VG_Clamp Output	Clamp Voltage Level			16.5		V
T_r	Output Rising Time	VDD = 16V, CL = 1nf		120		nSec
T_f	Output Falling Time	VDD = 16V, CL = 1nf		50		nSec
Over Temperature Protection						
I_RT	Output Current of RT pin	VDD = 16V, RI=100Kohm	70			uA
V_{TH}_OTP OTP	Threshold Voltage	VDD = 16V, RI=100Kohm	1.015	1.065	1.11 5	V
V_{TH}_OTP_off (Version V Only)	OTP Recovery Threshold Voltage	VDD = 16V, RI=100Kohm	1.16	5		V
V_{TH}_RT_latch (Version V Only)	RT Input Latch Threshold Voltage			0.6		V
T_D_OTP	OTP De-bounce Time	VDD = 16V, RI=100Kohm	100			uSec
V_RT_Open	RT Pin Open Voltage	VDD = 16V, RI=100Kohm	3.7			V
Frequency Shuffling						
Δf_OSC	Frequency Modulation range /Base frequency	RI=100Kohm -3			3	%
Freq_Shuffling	Shuffling Frequency	RI = 100Kohm		32		HZ

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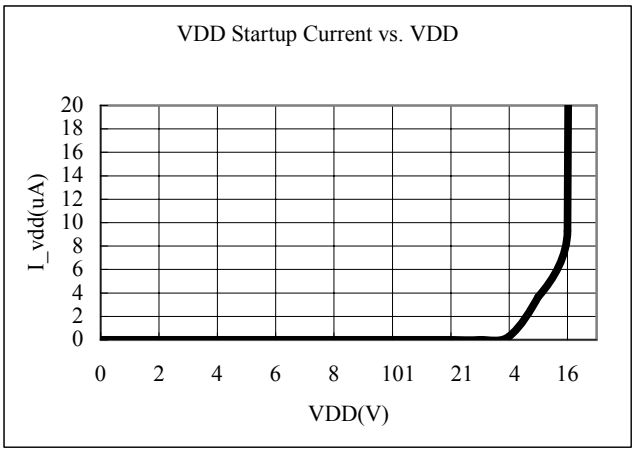
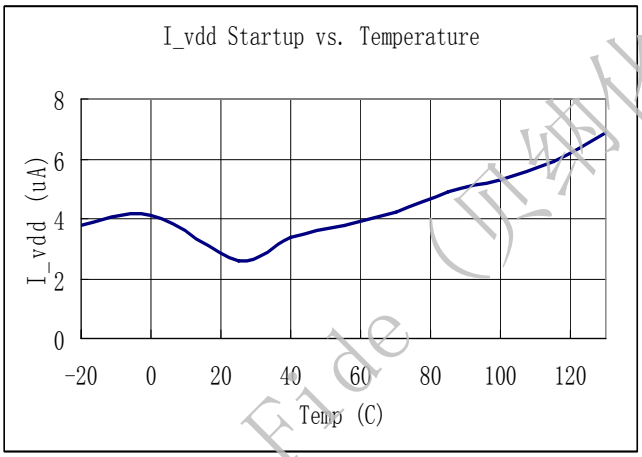
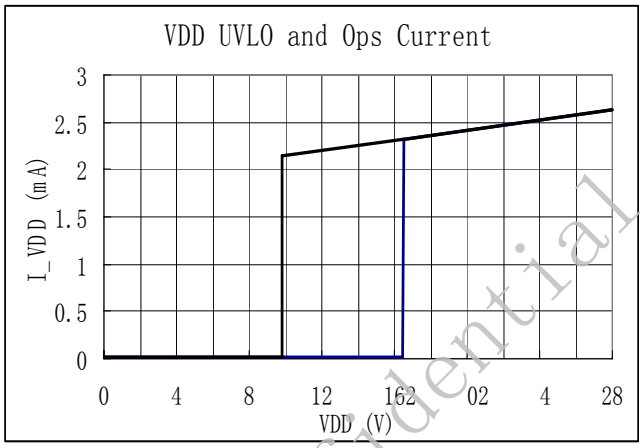
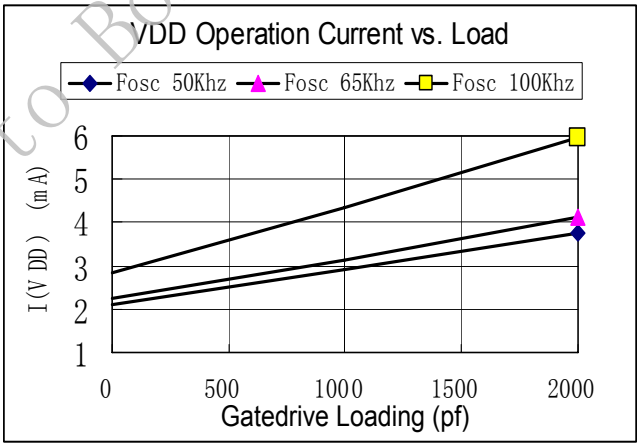
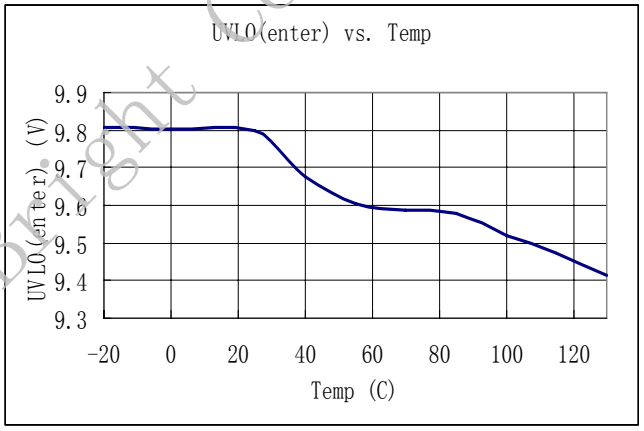
CHARACTERIZATION PLOTS

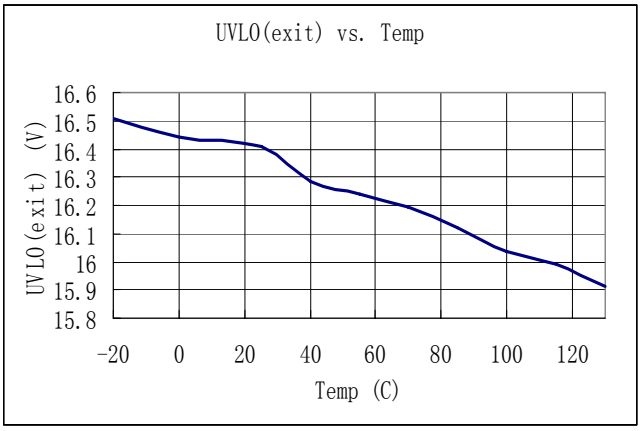












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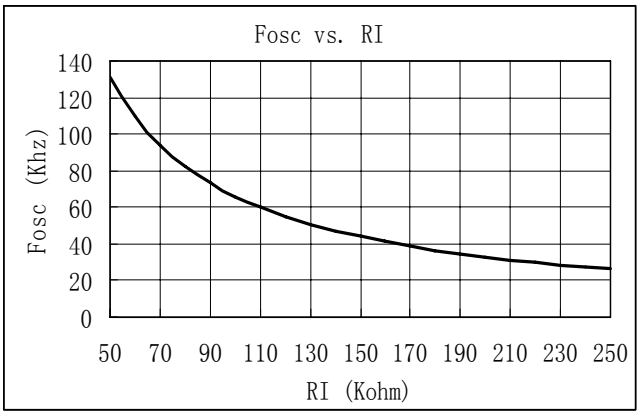

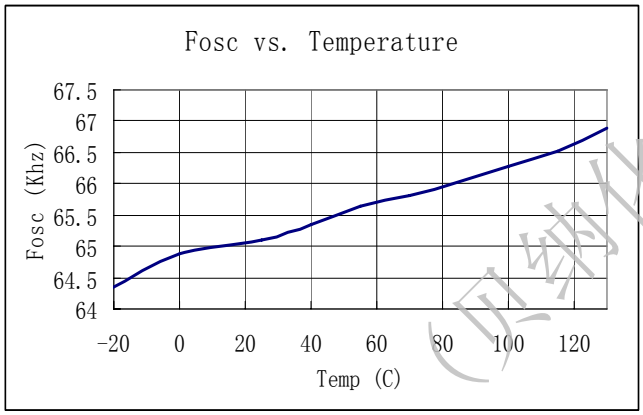

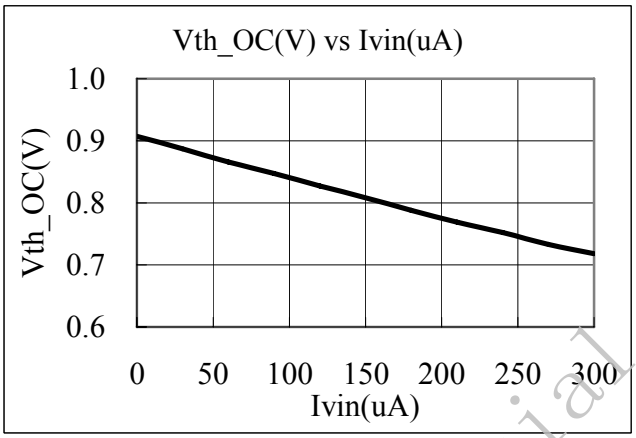

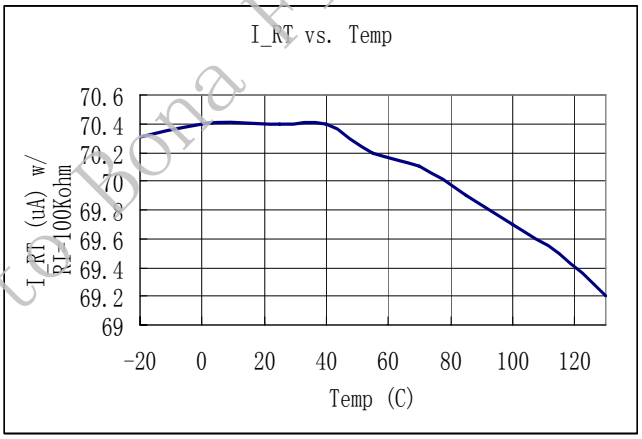

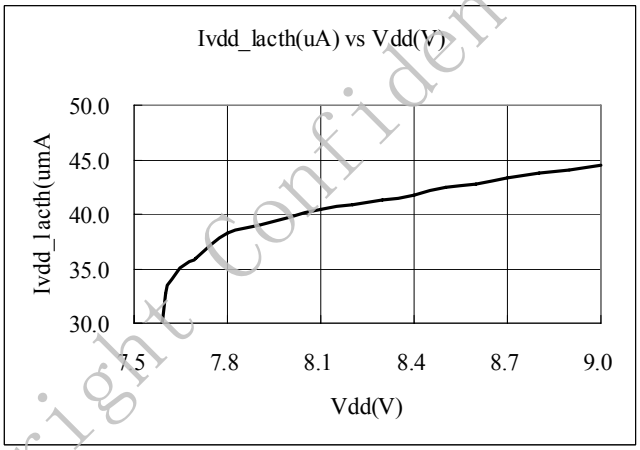

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OPERATION DESCRIPTION

OB2279 is a highl y integrated PWM controller IC optimized for offline flyback converter applications with requirement in latch shutdow n or auto recovery. The extended burst mode co ntrol greatl y reduces the standby powe r consum ption and helps the design easily meet the international power conservation requirements.

- **Startup Current and Start up Control**

Startup current of OB227 9 is designed to be ver y low so that VDD could be charged up above UVLO(exit) threshold lev el and device starts up quickly. A large value startup resistor can therefore be used to mini mize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, a 2 M Ω, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup a nd yet low power dissipation design solution.

- **Operating Current**

The Operating current of OB2279 is low at 2.3mA. Good efficiency is achieved with OB2279 low operating cu rrent together with extended burst mode control schemes.

- **Frequency shuffling for EMI improvement**

The frequency Shuffli ng/jittering (switching frequency m odulation) is implemented in OB2279. The oscillation frequenc y is m odulated with a internally generated random source so that the tone energy is eve nly spread out. The spread spectru m minimizes the conduction band EMI a nd therefore eases the sy stem design i n meeting str ingent EMI requirement.

- **Burst Mode Operation**

At zero load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on t he snubber cir cuit. The m agnitude of power loss is in propor tion to t he num ber of switching events within a fixed period of tim e. Reducing switching event s leads to th e reduction on the power loss and thus conserves the energy. OB2279 self adjusts the switching m ode according to the loading conditi on. At fro m no load to light/medium load conditi on, the FB input dro ps below burst mode thresh old level. D evice enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise th e gate drive re mains at off state to minimize the switching loss thus reduce the standby power consumption to the greatest extend. The nature of high f requency switching also reduces the audio noise at any loading conditions.

- **Oscillator Operation**

A resistor connected between RI and G ND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determ ined. The relationship between RI and switching frequenc y fol lows the belo w equation within the specified RI in Kohm range at nom inal loading operational condition.

$$F_{OSC} = \frac{6500}{RI(Kohm)}(Khz)$$

- **Current S ensing and Leading Edge Blanking (LEB)**

Cycle-by-Cycle current lim iting is offered in OB2279 curr ent m ode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber dio de reverse recovery so that the external RC filtering on sense input is no longer needed. The current lim it com parator is disabled and cannot t urn off the e xternal MOSFET duri ng the blanking period. Th e PWM duty c ycle is determined b y the current sense input voltage and the FB input voltage.

- **Internal Synchronized Slope Compensation**

Built-in slope com pensation circuit adds voltage ramp onto the current sense input voltag e for PWM generation. This greatly improves the close loop stability at CCM and pr events the sub-harm onic oscillation and thus reduces the output ripple voltage.

- **Over Temperature P rotection with Latch Shutdown(Only to T and L version)**

A NTC resi stor in series with a regular resistor should connect between RT and GND for temperature sensing and protection. NTC resi stor value becomes lower when the ambient temperature rises. With the fixed internal current I_{RT} flowing through the resistors, the voltage at RT pin becomes low er at high tem perature. The internal OTP circuit is trigge red and shutdown the MOSFET when the sensed input voltage is lower than V_{TH}_OTP.
OTP is a latched shutdown.

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- **RT Pin Used as Latch Shutdown Input Control**

RT pin could also be used as a control input to implement system latch shutdown function.
An example is to implement system OVP protection with a latch shutdown function through a photo coupler and affiliated circuits. When OVP detection signal connected to RT is lower than V_{TH}_OTP for Version T/L device, (or V_{TH}_OT_Latch for Version V), OB2279 controls system into latch shutdown. The recovery of the AC/DC system could only start by resetting internal latch when VDD voltage drops below VDD_De-latch value. This could be achieved by unplugging/re-plugging of AC source in AC start-up configuration.

- **Gate Drive**

OB2279 Gate is connected to the Gate of an external MOSFET for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI.
Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 16.5V clamp is added for MOSFET gate protection at higher than expected VDD input.

- **Protection Controls**

Good system reliability is achieved with OB2279's rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) with auto-recovery (V and T version) or latch shutdown(L version), over temperature protection (OTP) with auto-recovery (V version) or latch shutdown(T and L version), on-chip VDD over voltage protection (OVP) with latch shutdown and under voltage lockout (UVLO).
VDD OVP protection is a latched shutdown in OB2279.
The OCP threshold value is self adjusted lower at higher current into VIN pin. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage caused by inherent Over-Current sensing and control delay. A constant output power limit is achieved with recommended OCP compensation scheme.
At output overload condition, FB voltage is set higher. When FB input exceeds power limit threshold value for more than 80mS, control circuit reacts to turnoff the power MOSFET. This is so called OLP shutdown. It is either auto-recovery or latched shutdown depending on version of OB2279.
Similarly, control circuit shutdowns the power MOSFET when an Over Temperature condition is detected. This shutdown is either auto-recovery or latched depending on version of OB2279 been used.
VDD is supplied with transformer auxiliary winding output. It is clamped when VDD is higher than 35V. MOSFET is shut down when VDD drops below UVLO(enter) limit and device enters power on start-up sequence thereafter.

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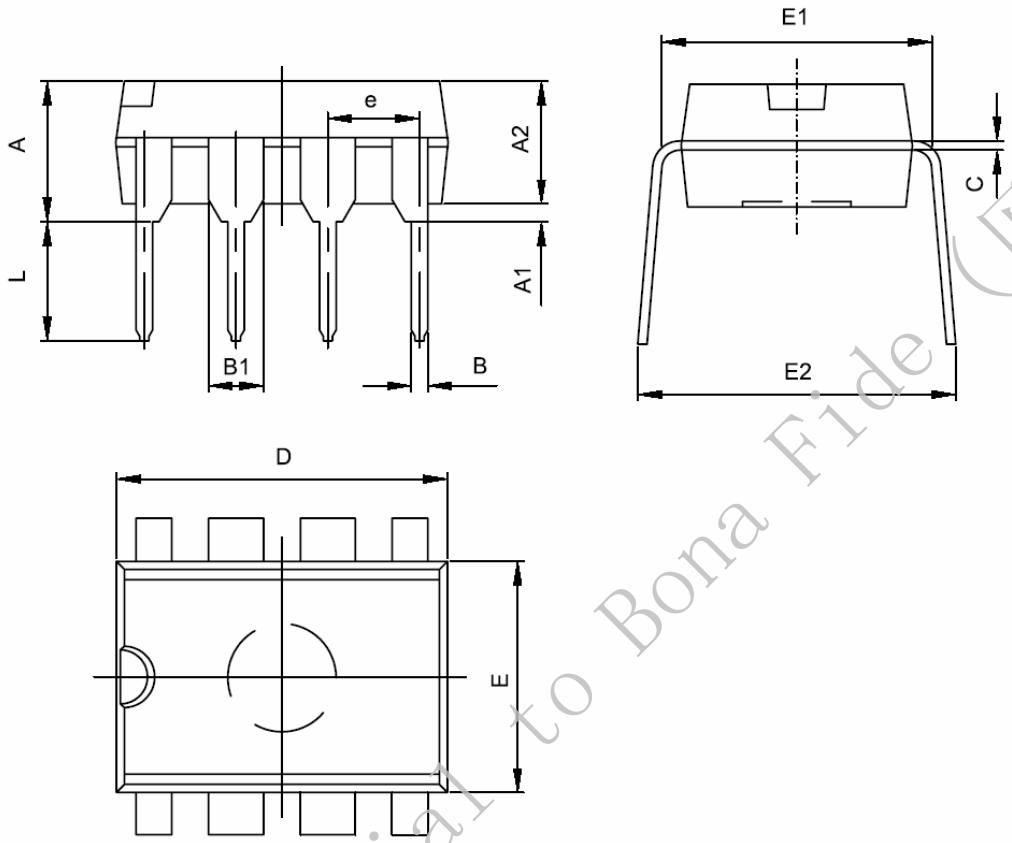
PACKAGE MECHANICAL DATA

8-Pin Plastic DIP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.360	0.560	0.014	0.022
B1	1.524(TYP)		0.060(TYP)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.620(TYP)		0.300(TYP)	
e	2.540(TYP)		0.100(TYP)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.400	0.323	0.370

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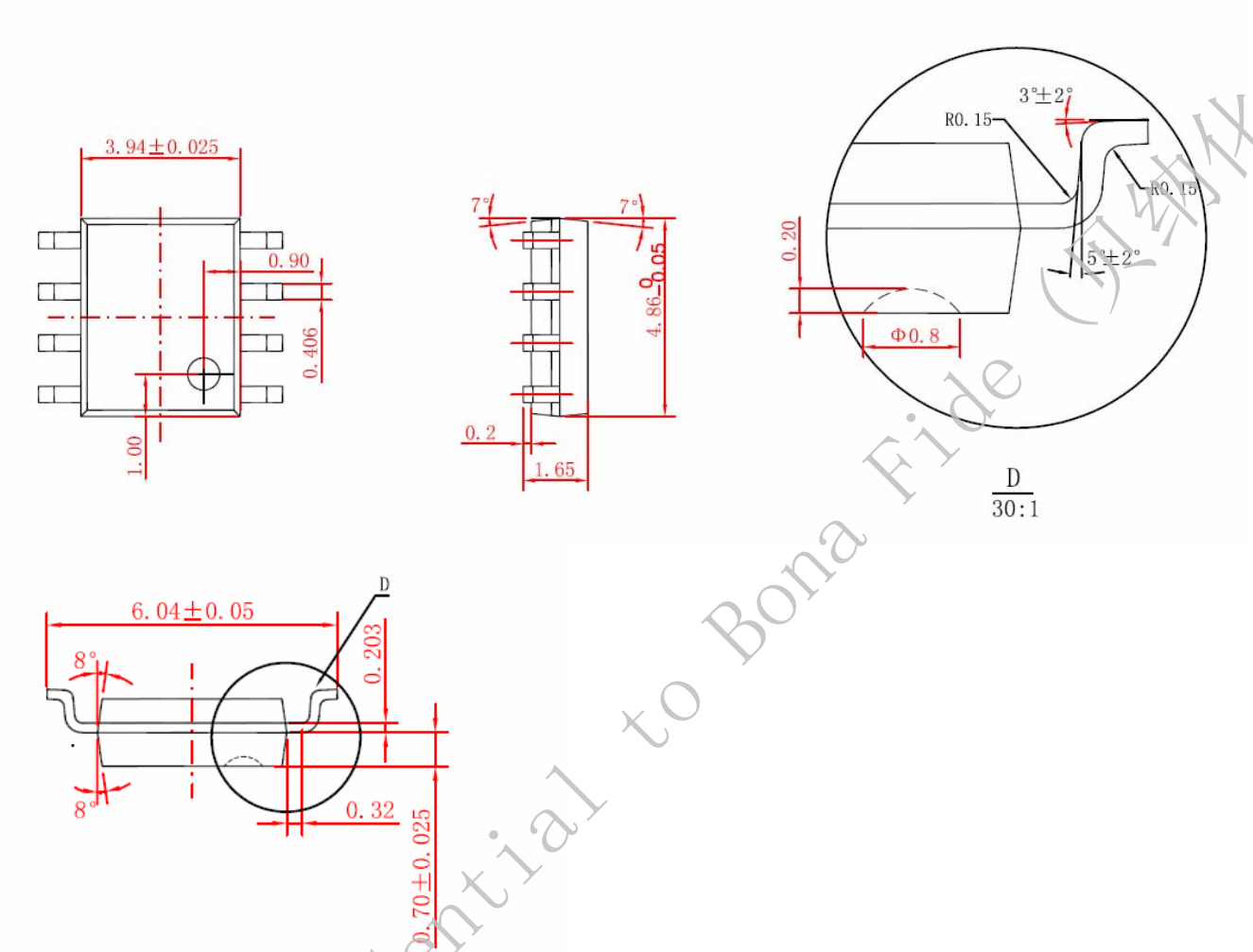
8-Pin Plastic SOP



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IMPORTANT NOTICE

RIGHT TO MAKE CHANGES

On-Bright Electronics Corp. reserves the right to make corrections, modifications, enhancements, improvements and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

WARRANTY INFORMATION

On-Bright Electronics Corp. warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with its standard warranty. Testing and other quality control techniques are used to the extent it deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

On-Bright Electronics Corp. assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using On-Bright 's components, data sheet and application notes. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

LIFE SUPPORT

On-Bright Electronics Corp.' s products are not designed to be used as components in devices intended to support or sustain human life. On-bright Electronics Corp. will not be held liable for any damages or claims resulting from the use of its products in medical applications.

MILITARY

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