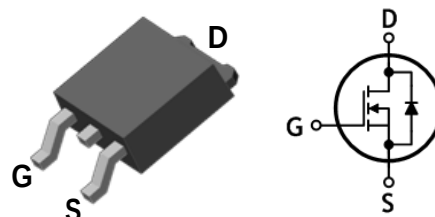


SWITCHING REGULATOR APPLICATION

Features

- High voltage: $BV_{DSS}=250V$ (Min.)
- Low gate charge: $Q_g=14.5nC$ (Typ.)
- Low drain-source On resistance: $R_{DS(on)}=0.43\Omega$ (Max.)
- RoHS compliant device
- Halogen free package

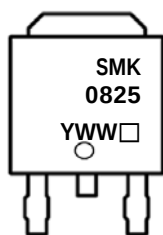


TO-252

Ordering Information

Part Number	Marking	Package
SMK0825D	SMK0825	TO-252

Marking Information



Column 1, 2: Device Code
 Column 3: Production Information
 e.g.) YWW□
 -. YWW: Date Code (year, week)
 -. □: Factory Code ('A': AUK, 'S': SP Semi.)

Absolute maximum ratings ($T_C=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	250	V
Repetitive Avalanche Voltage (Note 1, 2)	$V_{DS(Avalanche)}$	300	V
Gate-source voltage	V_{GSS}	± 30	V
Drain current (DC) *	I_D	$T_C=25^\circ C$	8 A
		$T_C=100^\circ C$	5.2 A
Drain current (Pulsed) *	I_{DM}	32	A
Single pulsed avalanche energy (Note 2)	E_{AS}	356	mJ
Repetitive avalanche current (Note 1)	I_{AR}	8	A
Repetitive avalanche energy (Note 1)	E_{AR}	7.4	mJ
Power dissipation	P_D	48	W
Junction temperature	T_J	150	$^\circ C$
Storage temperature range	T_{stg}	-55~150	$^\circ C$

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 2.6	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 50	

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	250	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	2	-	4	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=250\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=4\text{A}$	-	0.35	0.43	Ω
Internal gate resistance	R_G	$f=1\text{MHz}$, $V_{DS}=0\text{V}$	-	4	10	Ω
Forward transfer conductance (Note 3)	g_{fs}	$V_{DS}=10\text{V}$, $I_D=4\text{A}$	-	7	-	S
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	619	773	pF
Output capacitance	C_{oss}		-	141	176	
Reverse transfer capacitance	C_{rss}		-	33	41	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DD}=125\text{V}$, $I_D=8\text{A}$ $R_G=25\Omega$	11	15	35	ns
Rise time (Note 3,4)	t_r		32	85	115	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		62	90	135	
Fall time (Note 3,4)	t_f		41	65	98	
Total gate charge (Note 3,4)	Q_g	$V_{DS}=200\text{V}$, $V_{GS}=10\text{V}$ $I_D=8\text{A}$	-	14.5	18.2	nC
Gate-source charge (Note 3,4)	Q_{gs}		-	4	-	
Gate-drain charge (Note 3,4)	Q_{gd}		-	4.5	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	8	A
Source current (Pulsed)	I_{SM}		-	-	32	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=8\text{A}$	-	-	1.4	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_S=8\text{A}$, $V_{GS}=0\text{V}$ $dI_F/dt=100\text{A}/\mu\text{s}$	-	178	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	1.16	-	μC

Note:

1. Repeated rating: Pulse width limited by maximum junction temperature
2. $L=8.9\text{mH}$, $I_{AS}=8\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Electrical Characteristic Curves

Fig. 1 $I_D - V_{DS}$

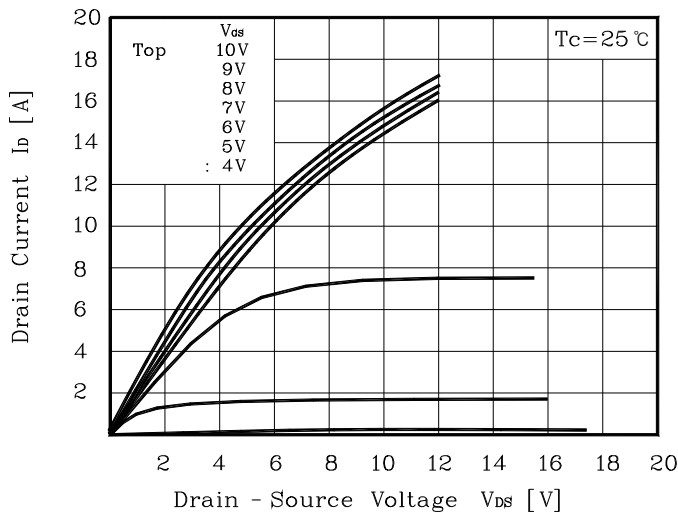


Fig. 2 $I_D - V_{GS}$

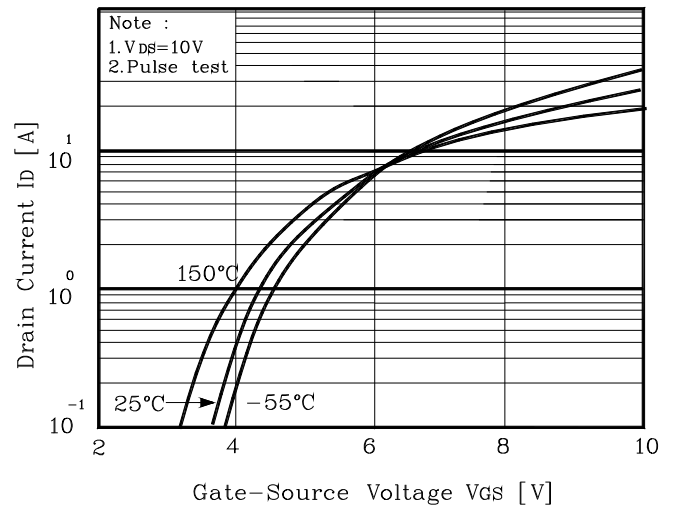


Fig. 3 $R_{DS(ON)} - I_D$

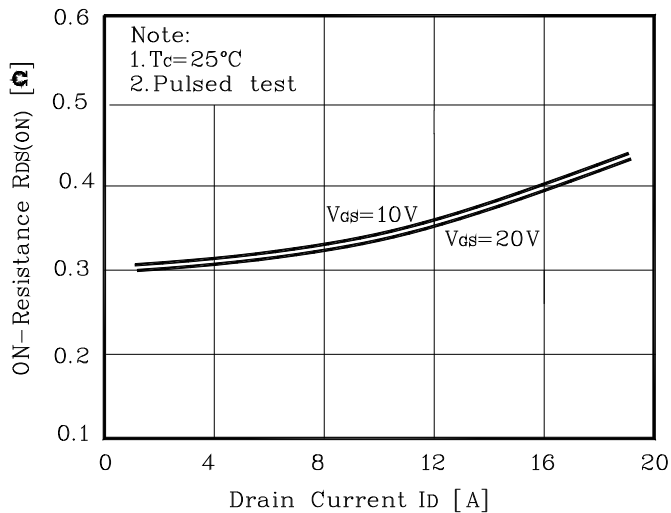


Fig. 4 $I_S - V_{SD}$

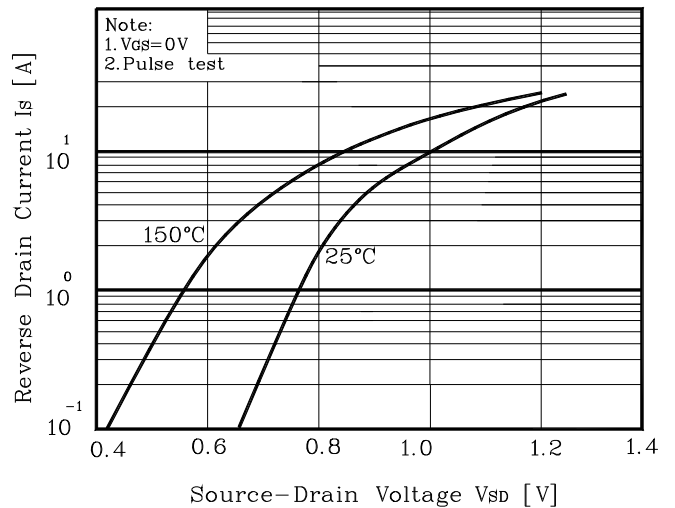


Fig. 5 Capacitance - V_{DS}

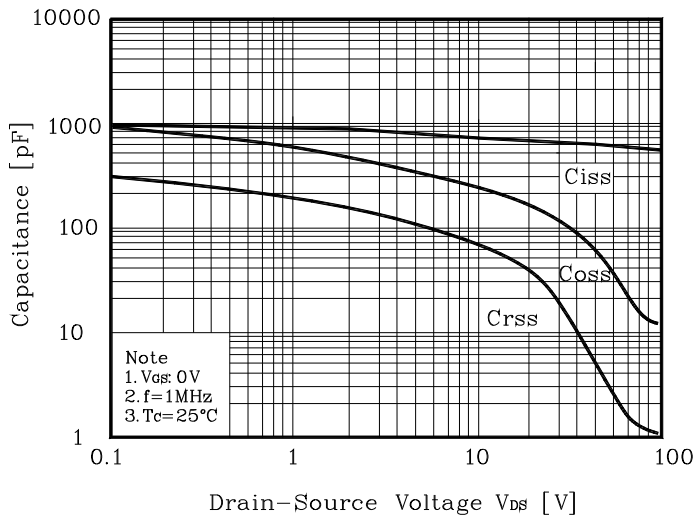
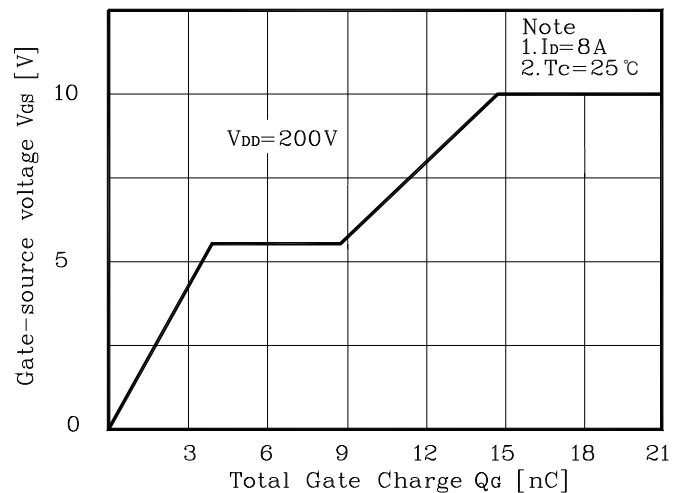


Fig. 6 $V_{GS} - Q_G$



Electrical Characteristic Curves (Continue)

Fig. 7 $V_{DS} - T_J$

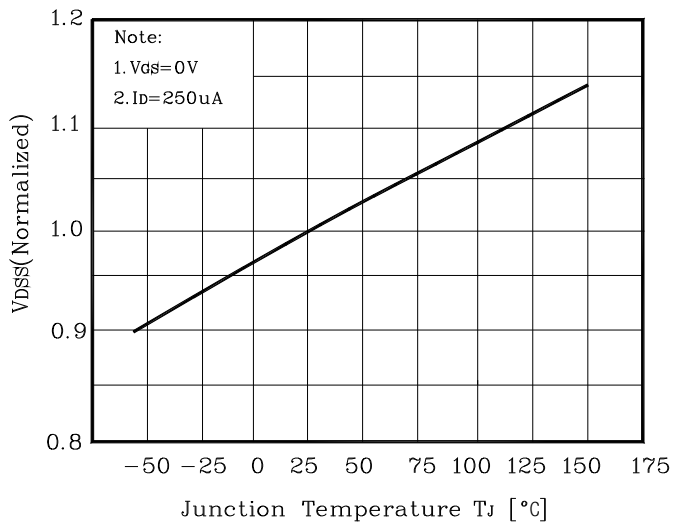


Fig. 8 $R_{DS(on)} - T_J$

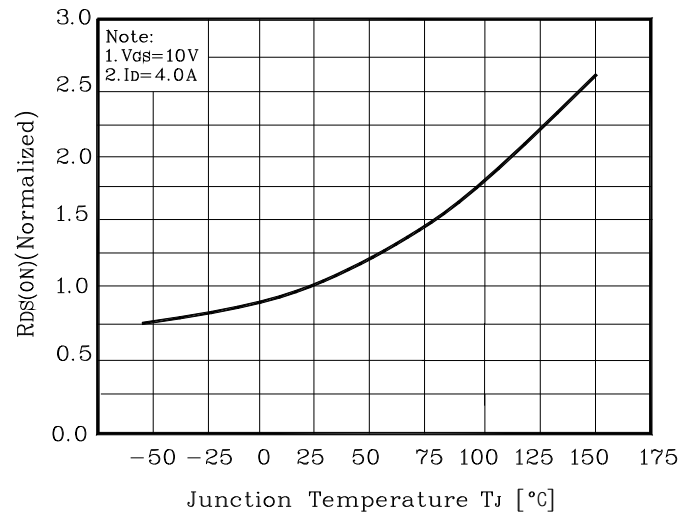


Fig. 9 $I_D - T_C$

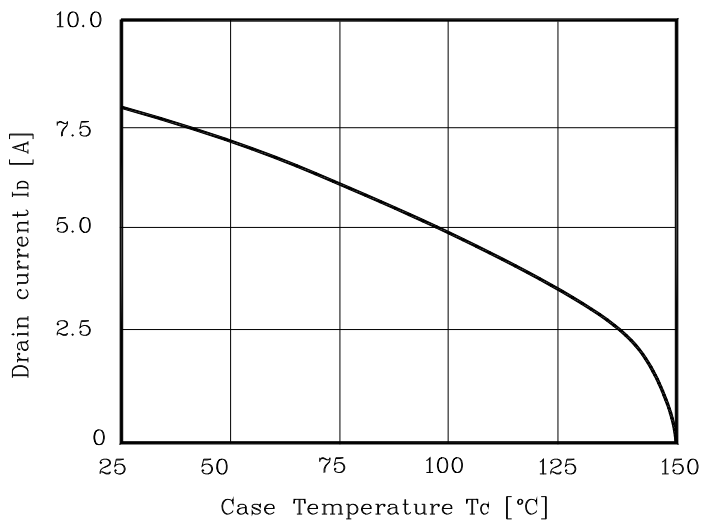


Fig. 10 Safe Operating Area

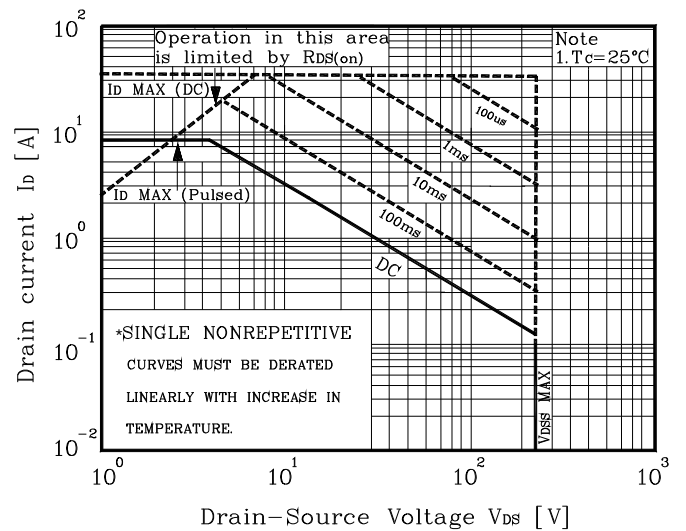


Fig. 11 Gate Charge Test Circuit & Waveform

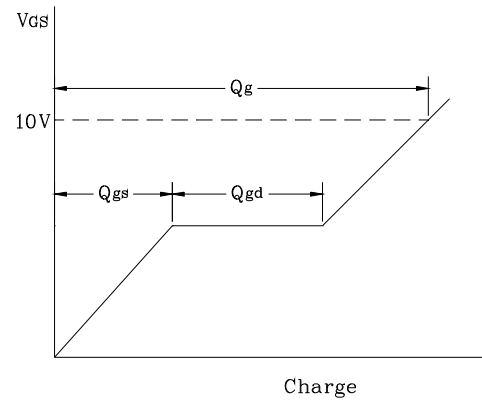
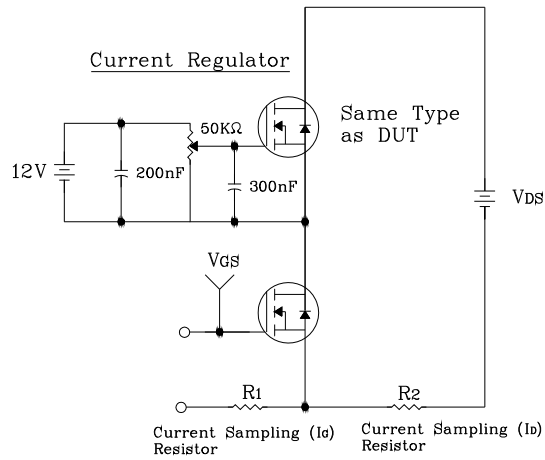


Fig. 12 Resistive Switching Test Circuit & Waveform

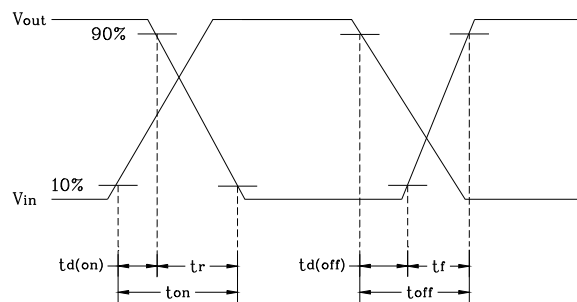
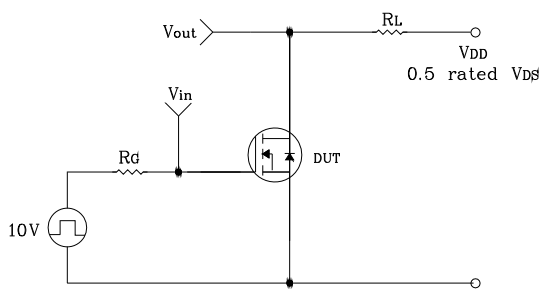


Fig. 13 E_{AS} Test Circuit & Waveform

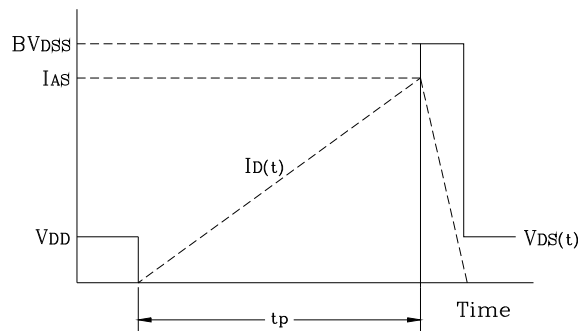
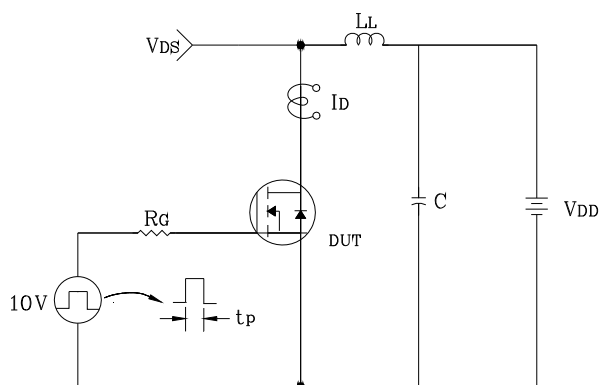
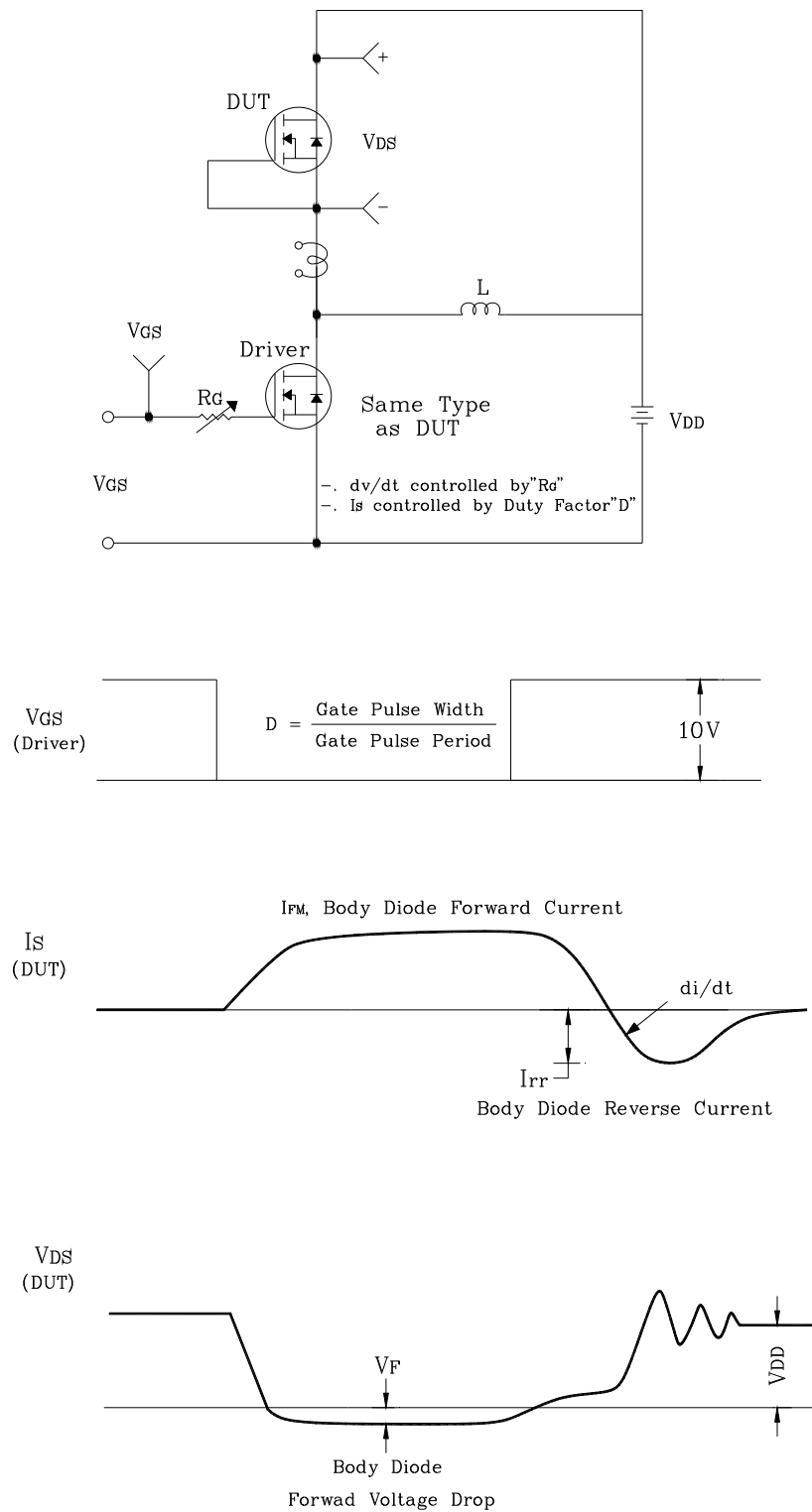
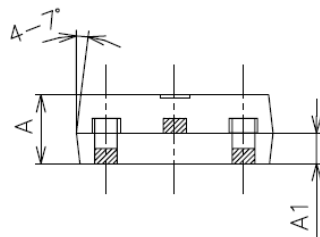
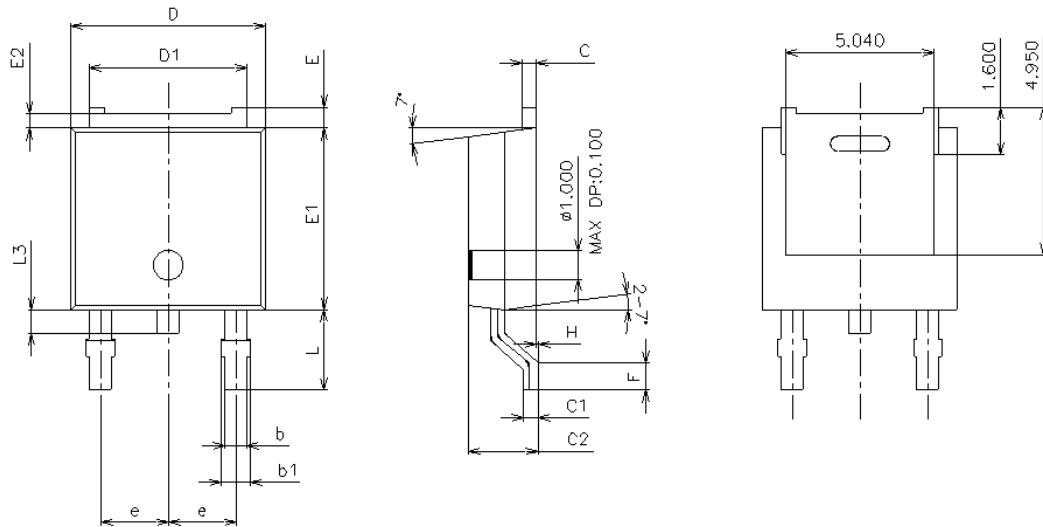


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform

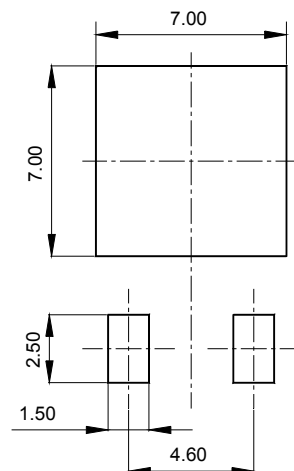


Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
D	6.40	6.60	6.80	
D1	5.14	5.34	5.54	
E	0.50	0.70	0.90	
E1	5.90	6.10	6.30	
E2	0.50 TYP			
A	2.20	2.30	2.40	
A1	0.87	1.07	1.27	
C	0.40	0.50	0.60	
C1	0.40	0.50	0.60	
C2	2.10	2.30	2.50	
L	2.50	2.70	2.90	
L3	0.60	0.80	1.00	
b	0.66	0.76	0.86	
b1	0.96 MAX			
e	2.10	2.30	2.50	
F	0.80 MIN			
H	0.00	-	0.10	

Recommended Land Pattern [unit: mm]



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